In the Claims

1. (original) An in-process semiconductor device comprising:

at least two columns of transistors within a single sector of a memory device, each transistor having a source region;

a dielectric layer having an opening therein, said opening defined by first and second cross sectional sidewalls of said dielectric layer, wherein each said first and second sidewall overlies one said column of transistors;

first and second dielectric spacers, wherein each said first and second spacer covers one said sidewall of said dielectric layer; and

a conductive line partially formed between said two columns of transistors and partially formed in said opening in said dielectric layer between said first and second dielectric sidewalls, wherein said spacers separate said conductive line from physical contact with said dielectric layer, and wherein said conductive line electrically couples each said source region of each said transistor in each of said two columns of transistors.

2. (original) The in-process semiconductor device of claim 1 wherein said dielectric layer is a first dielectric layer and said semiconductor device further comprises a second dielectric layer overlying and contacting said first dielectric layer, said second dielectric layer having an opening therein defined by first and second cross sectional sidewalls of said second dielectric layer, said first and second cross sectional sidewalls of said second dielectric layer being continuous with said first and second cross sectional sidewalls of said first dielectric layer, and wherein each said first and second spacer covers one said sidewall of said second dielectric layer, and wherein said conductive line is partially formed in said opening in said second dielectric layer between said first and second sidewalls of said second dielectric layer, and wherein said spacers separate said conductive line from physical contact with said second dielectric layer.

3. (original) The in-process semiconductor device of claim 2 wherein each said transistor further comprises a dielectric capping layer.

4. (original) The in-process semiconductor device of claim 3 wherein said second dielectric layer, said spacers covering said first and second sidewalls of said first dielectric layer, and said spacers covering said first and second sidewalls of said second dielectric layer each comprise silicon nitride.

5. (presently amended) An in-process semiconductor device comprising:

at least a first transistor and a second transistor sharing a common source region, with each transistor comprising a control gate;

a capping layer covering said first and second transistor control gates, said capping layer having a horizontally-oriented upper surface;

a gate oxide layer extending from under said control gate of said first transistor control gate, to under said second transistor control gate;

a first spacer contacting said first transistor control gate and a second spacer contacting said second transistor control gate;

a blanket etch-resistant layer which contacts said gate oxide layer at a location between said first and second transistors, and which contacts said capping layer and said first and second spacers, and which overlies both said first and second transistor control gates;

a dielectric layer which contacts said blanket etch-resistant layer at said location between said first and second transistors, said dielectric layer comprising:

a first upper surface which is at a level below said horizontally-oriented upper surface of said capping layer;

a second upper surface which is at a level above said horizontally-oriented upper surface of said capping layer;

a first vertically-oriented sidewall which overlies said first transistor control gate; and

a second vertically-oriented sidewall which overlies said second transistor control gate,

wherein a portion of said etch-resistant layer between said first and second sidewalls is not covered by said dielectric layer.

6. (original) The in-process device of claim 5 further comprising an unetched spacer layer which contacts said first and said second sidewalls and first upper surface of said dielectric layer.

7. (original) The in-process device of claim 5 further comprising:

a first spacer which contacts said first vertically-oriented sidewall of said dielectric layer; and

a second spacer which contacts said second vertically-oriented sidewall of said dielectric layer,

wherein said first upper surface of said dielectric layer is exposed.

8. (original) An in-process semiconductor device comprising:

a semiconductor wafer;

at least a first word line which defines control gates for a plurality of transistors in a first column and a second word line which defines control gates for a plurality of transistors in a second column, each word line overlying said semiconductor wafer;

a source diffusion region within said semiconductor wafer;

a gate oxide layer which extends from under said first word line, across said source diffusion region, to under said second word line;

a first spacer which contacts said first word line and a second spacer which contacts said second word line;

an etch-resistant layer which contacts said first spacer, said second spacer, and said gate oxide layer and which defines a recess over said source diffusion region;

a dielectric layer formed within said recess over said source diffusion region; and

an etch mask having an opening therein which exposes said dielectric layer.

9. (original) The in-process semiconductor device of claim 8 further comprising a plurality of floating gates with each floating gate associated with one of said plurality of transistors in said first and second columns of transistors.

10. (original) The in-process semiconductor device of claim 8 further comprising a first capping layer on said first word line and a second capping layer on said second word line, wherein said etch-resistant layer does not contact at least a portion of an upper surface of said first and second capping layers.

11. (original) The in-process semiconductor device of claim 8 further comprising:

first a drain diffusion region within said semiconductor wafer at a location lateral to said first word line and a second drain diffusion region within said semiconductor wafer at a location lateral to said second word line, wherein said source diffusion region is interposed between said first and second drain diffusion regions;

said dielectric layer formed at locations over said first and second drain diffusion regions; and

said etch mask overlying said dielectric layer over said first and second drain diffusion regions such that said dielectric layer, at said locations over said first and second drain diffusion regions, is not exposed.